ABSTRACT OF THE DISCLOSURE

In a nonvolatile semiconductor memory device, a voltage Vpp of 12 V applied to an external terminal is dropped by a resistance element of 3500 Ω to a voltage Vrpin. Vrpin is inputted to a regulator circuit to output a stabilized voltage Vpll of 5 V, so that Vpll is applied to a common source line as an erase pulse voltage. Termination of a first erase pulse application is judged by a level detection circuit based on a result of comparison between a reference voltage Vref of 11 V and an input voltage Vrpin which begins with 5 V upon start of the erase operation. Thus, since a large voltage magnitude of the input voltage is secured, a variation in the threshold voltage of a memory cell after the termination of the first erase pulse application can be made small, thereby preventing degradation of the erase speed.